Low-Cost & Design-flexible 3D-IC Packaging Solutions

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Challenges of Today

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Cost

Moore's law slows down while costs continue to increase

Performance

Power efficiency and bandwidth are limited by physical constraint

Memory BW

Bottle-neck of system performance is memory bandwidth

- Our answer to today’s challenges is 3D ICs and Advanced Packaging

Trend of Die & PKG Designs

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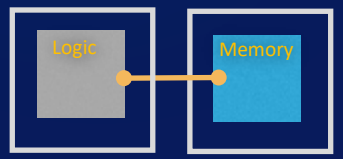
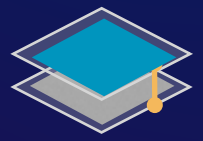
Mobile Design

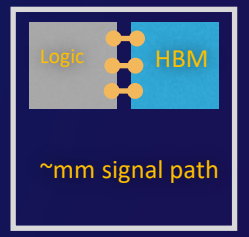


~cm signal path

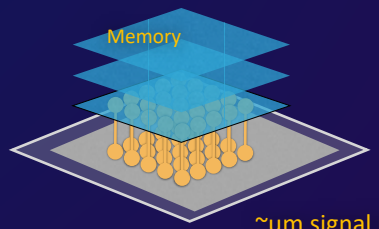


Package-on-Package

Processor-Memory Bandwidth

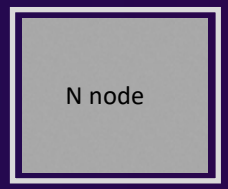


~mm signal path

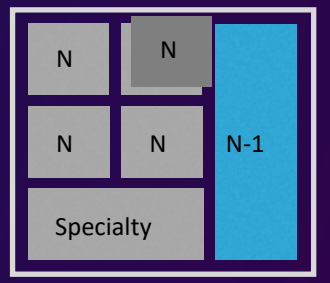


~um signal path

Heterogeneous Integration

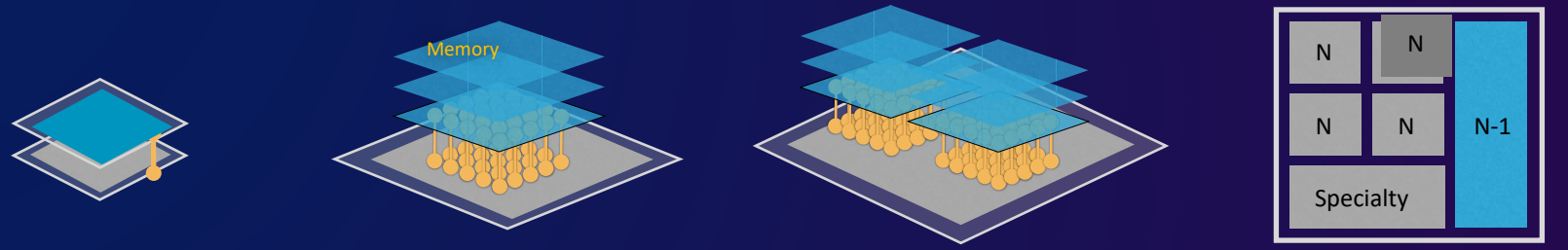


chiplets



- Die/PKG designs are moving to 3D for performance and yield improvement
  - Closer Proximity, Wider Bandwidth, Higher number of dies/chiplets
- The design granule for 3D is getting smaller
  - Packaged-Device level → die level → block level (Chiplets) → IP level

Challenges for Wide-spread Use of 3D ICs & Adv. PKG



Complex Design	Multi-physics Analysis	Long NPI Time	High PKG Cost
Bigger and finer PKG Multiple chiplets Interposer TSVs Integrated Passives	Thermal Mechanical Electrical	Yield improvement time (test vehicles)	Bigger PKG Expensive Si-interposer Fab processing

- 3D ICs will bring enormous innovations to the semiconductors
- However, we need solutions to overcome the challenges in 3D ICs

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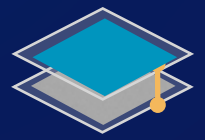
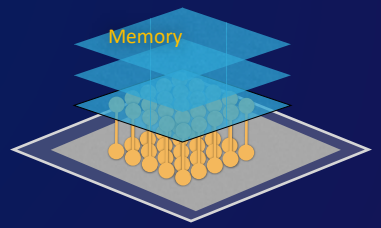
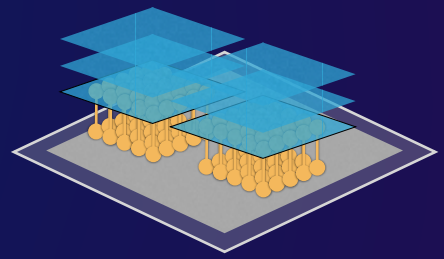
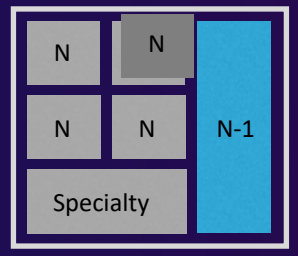
Wishes for EDAs









Complex Design

Bigger and finer PKG
Multiple chiplets
Interposer
TSVs
Passives

Multi-physics Analysis

Thermal
Mechanical
Electrical

Long NPI Time

Yield improvement time
(test vehicles)

High PKG Cost

Bigger PKG
Expensive Si-interposer
Fab processing

- EDA tools that can make complex designs simpler
- Multi-physics analysis tools that can help reduce the analysis and yield improvement time

Our Heterogeneous Integration Platforms

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Foundry

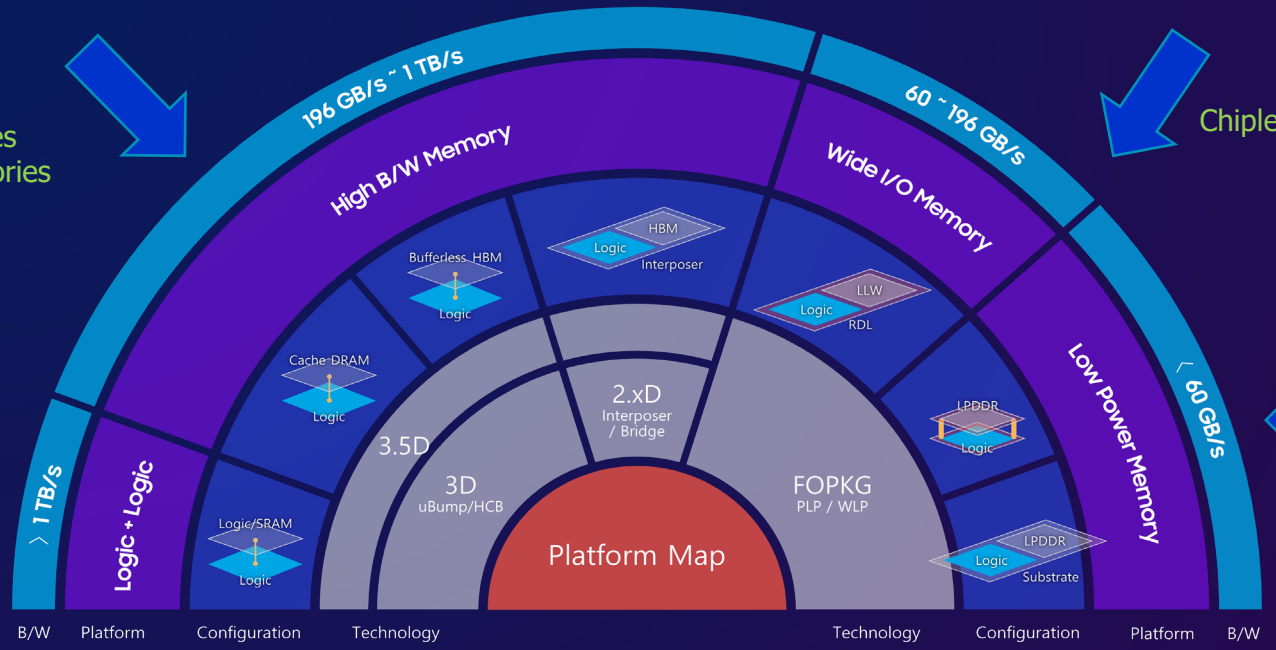
Memory

Fabless

Customized dies

Standard Memories
Customized memories

Chiplets



Integrated design solutions

- ISC (Integrated Silicon/Stack Cap)
- IVR (Integrated Voltage Reg.)

- Goals to achieve
  - High performance
  - Lower total cost
  - Higher power efficiency
  - Higher memory bandwidth

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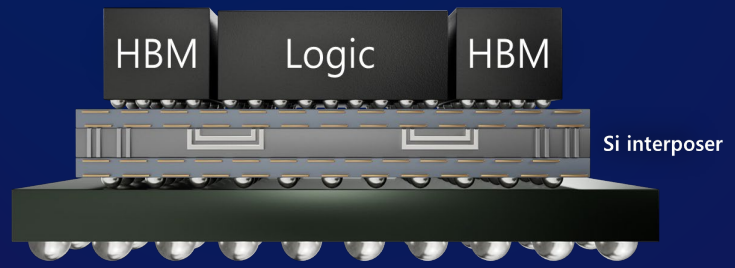
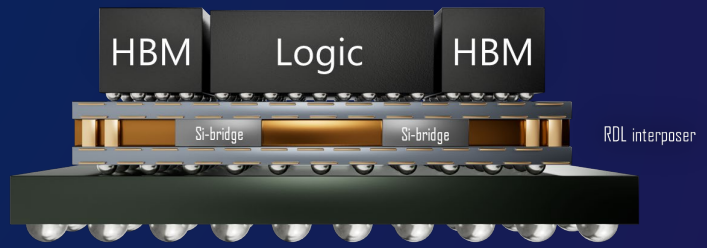
Cost-effective AI/HPC Package Platforms

Si-interposer



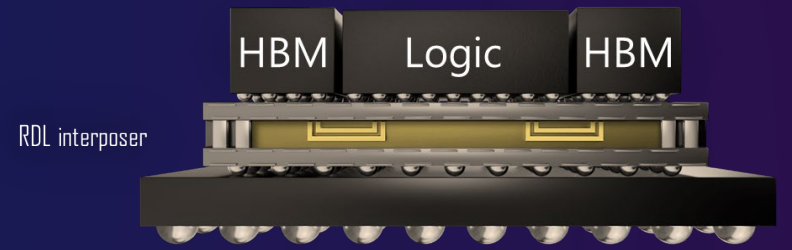
Silicon Interposer + ISC
Line/Space = 0.4/0.4 um

RDL interposer/Si-bridge



Silicon bridge + ISC
Line/Space = 0.4/0.4 um
Panel-Level RDL interposer

RDL interposer



Panel-Level RDL interposer
Line/Space = 5/5 um

Down to 22% vs Si-interposer (12x HBM)
Package cost

≥ 4x Reticle
Size expansion

Same vs Si-interposer
Signal/Power Integrity

- Panel-level RDL interposer enables larger interposer, more HBMs and multi-dies for AI/Data-center applications
- Using Panel-level Packaging, we can lower the package cost and support bigger package size

Summary

- Our answer to today's challenges is 3D ICs and Advanced Packaging
  - Cost, Performance and Memory BW
- However, we need solutions to overcome the challenges for wide-spread use of 3D ICs
  - Design is complex
  - Analysis needs to consider multi-physics at the same time
  - Long yield improvement time by using test vehicles
  - High cost by using fab processing and expensive Si-interposer
- We are developing cost-effective and design-flexible packaging solutions for wide-spread use of 3D ICs that will boost the industry's innovation
  - Finer-pitch uBump and Bump-less 3D stacking
  - Panel-level based RDL interposer for AI/HPC applications
  - Integrated design solutions